Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 23, 25, 81-89, amend claims 1, 4-6, 11-12, 15-22, 24, 26-28, 30-44, 46-60, 62-80 as follows:

Listing of Claims:

1. (Currently Amended) An integrated circuit package assembly for electrically isolating modules, comprising:

a substrate having a first side and an opposing second side;

a first module attached to the first side of the substrate;

a second module attached to the first side of the substrate;

a first conductive surface proximate to the second side of the substrate~~, the first conductive surface conductively~~ and coupled to the first module; and

a second conductive surface coupled to the second module and spaced apart from the first conductive surface to capacitively couple signals communicated between the first and second modules. ~~form a capacitor with the first conductive surface, the second conductive surface being coupled to the second module.~~

2. (Original) The package assembly of claim 1, further comprising a dielectric interposed between the first and second conductive surfaces.

3. (Original) The package assembly of claim 1, further comprising an encapsulation substantially surrounding the package assembly.

4. (Currently Amended) The package assembly of claim 3 wherein the encapsulation ~~package assembly is encased in~~ further comprises a polymer.

5. (Currently Amended) The package assembly of claim 3 wherein the encapsulation ~~package assembly is encased in~~ comprises a ceramic.

6. (Currently Amended) The package assembly of claim 3 wherein the encapsulation ~~package assembly is encased in~~ comprises a glass.

7. (Original) The package assembly of claim 1 wherein the first module is an integrated circuit.

8. (Original) The package assembly of claim 7 wherein the integrated circuit is a physical layer chip.

9. (Original) The package assembly of claim 1 wherein the second module is an integrated circuit.

10. (Original) The package assembly of claim 9 wherein the integrated circuit is a link layer chip.

11. (Currently Amended) The package assembly of claim 1, further comprising a resistor having a first terminal coupled to the first conductive surface and ~~further having~~ a second terminal coupled to the second conductive surface.

12. (Currently Amended) The package assembly of claim ~~10~~ 11 wherein the resistor has a resistance of approximately one megohm.

13. (Original) The package assembly of claim 11 wherein the resistor is a resistant film.

14. (Original) The package assembly of claim 1, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

15. (Currently Amended) The package assembly of claim ~~13~~ 14 wherein the first ground plane comprises a ground wire of a cable bus.

16. (Currently Amended) The package assembly of claim ~~13~~ 14 wherein the second ground plane comprises a chassis of a computer.

17. (Currently Amended) An integrated circuit package assembly for electrically isolating integrated circuits within a module, comprising:

a substrate having a first side and an opposing second side;

a module attached to the first side of the substrate, the module having a first and second integrated circuit;

a first conductive surface proximate to the second side of the substrate, the first conductive surface conductively coupled to the first integrated circuit; and

a second conductive surface coupled to the second integrated circuit and spaced apart from the first conductive surface, the first conductive surface and the second conductive surface being configured to capacitively exchange signals between the first integrated circuit and the second integrated circuit. ~~to form a capacitor with the first conductive surface, the second conductive surface being conductively coupled to the second integrated circuit.~~

18. (Currently Amended) The package assembly of claim ~~16~~ 17, further comprising a dielectric interposed between the first and second conductive surfaces.

19. (Currently Amended) The package assembly of claim ~~16~~ 17, further comprising an encapsulation substantially surrounding the package assembly.

20. (Currently Amended) The package assembly of claim ~~18~~ 19 wherein the encapsulation ~~package assembly is encased in~~ comprises a polymer.

21. (Currently Amended) The package assembly of claim ~~18~~ 19 wherein the encapsulation ~~package assembly is encased~~ comprises a ~~in~~ ceramic.

22. (Currently Amended) The package assembly of claim ~~18~~ 19 wherein the encapsulation ~~package assembly is encased in~~ comprises a glass.

23. (Cancelled)

24. (Currently Amended) The package assembly of claim ~~22~~ 17 wherein the first integrated circuit is a physical layer chip.

25. (Cancelled)

26. (Currently Amended) The package assembly of claim ~~24~~ 17 wherein the second integrated circuit is a link layer chip.

27. (Currently Amended) The package assembly of claim ~~16~~ 17, further comprising a resistor having a first terminal coupled to the first conductive surface and ~~further having~~ a second terminal coupled to the second conductive surface.

28. (Currently Amended) The package assembly of claim ~~26~~ 27 wherein the resistor has a resistance of approximately one megohm.

29. (Original) The package assembly of claim 27 wherein the resistor is a resistant film.

30. (Currently Amended) The package assembly of claim ~~16~~ 17, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

31. (Currently Amended) The package assembly of claim ~~28~~ 30 wherein the first ground plane comprises a ground wire of a cable bus.

32. (Currently Amended) The package assembly of claim ~~28~~ 30 wherein the second ground plane comprises a chassis of a computer.

33. (Currently Amended) An integrated circuit package assembly for electrically isolating modules, comprising:

a first substrate with a first and opposing second side and having a first module attached to the first side;

a first conductive surface proximate to the second side of the first substrate, the first conductive surface being conductively coupled to the first module;

a second substrate with a first and opposing second side and having a second module attached to the first side; and

a second conductive surface proximate to the ~~opposing~~ second side of the second substrate, the second conductive surface being conductively coupled to the second module and spaced apart from the first conductive surface to capacitively couple signals between the first module and the second module. ~~form a capacitor with the first conductive surface.~~

34. (Currently Amended) The package assembly of claim ~~31~~ 33, further comprising a dielectric interposed between the first and second conductive surfaces.

35. (Currently Amended) The package assembly of claim ~~31~~ 33, further comprising an encapsulation substantially surrounding the package assembly.

36. (Currently Amended) The package assembly of claim ~~33~~ 35 wherein the encapsulation ~~package assembly is encased in~~ comprises a polymer.

37. (Currently Amended) The package assembly of claim ~~33~~ 35 wherein the encapsulation ~~package assembly is encased in~~ comprises a ceramic.

38. (Currently Amended) The package assembly of claim ~~33~~ 35 wherein the encapsulation ~~package assembly is encased in~~ comprises a glass.

39. (Currently Amended) The package assembly of claim ~~31~~ 33 wherein the first module ~~is~~ comprises an integrated circuit.

40. (Currently Amended) The package assembly of claim ~~37~~ 39 wherein the integrated circuit ~~is~~ comprises a physical layer chip.

41. (Currently Amended) The package assembly of claim ~~31~~ 33 wherein the second module ~~is~~ comprises an integrated circuit.

42. (Currently Amended) The package assembly of claim ~~39~~ 41 wherein the integrated circuit ~~is~~ comprises a link layer chip.

43. (Currently Amended) The package assembly of claim ~~31~~ 33, further comprising a resistor having a first terminal coupled to the first conductive surface and ~~further having~~ a second terminal coupled to the second conductive surface.

44. (Currently Amended) The package assembly of claim ~~41~~ 43 wherein the resistor has a resistance of approximately one megohm.

45. (Original) The package assembly of claim 43 wherein the resistor is a resistant film.

46. (Currently Amended) The package assembly of claim ~~31~~ 33, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

47. (Currently Amended) The package assembly of claim ~~43~~ 46 wherein the first ground plane comprises a ground wire of a cable bus.

48. (Currently Amended) The package assembly of claim ~~43~~ 46 wherein the second ground plane comprises a chassis of a computer.

49. (Currently Amended) An integrated circuit package assembly for electrically isolating integrated circuits within a module, comprising:

a substrate;

a first module having a first and an opposing second side, the first side of the first module being attached to the substrate ~~on the first side~~;

a second module having a first and an opposing second side, the first side of the second module being attached to the substrate ~~on the first side~~;

a non-conductive layer having a first and opposing second side, the first side of the non-conductive layer being proximate to the ~~opposing~~ second sides of the first and second modules;

a first conductive surface proximate to the second side of the first non-conductive layer, the first conductive surface conductively coupled to the first module; and

a second conductive surface conductively coupled to the second module and spaced apart from the first conductive surface, the first conductive surface and the second conductive surface being configured to capacitively couple signals between the first module and the second module. ~~to form a capacitor with the first conductive surface, the second conductive surface being conductively coupled to the second module.~~

50. (Currently Amended) The package assembly of claim ~~46~~ 49, further comprising a dielectric interposed between the first and second conductive surfaces.

51. (Currently Amended) The package assembly of claim ~~46~~ 49, further comprising an encapsulation substantially surrounding the package assembly.

52. (Currently Amended) The package assembly of claim ~~48~~ 51 wherein the encapsulation ~~package assembly is encased in~~ comprises a polymer.

53. (Currently Amended) The package assembly of claim ~~48~~ 51 wherein the encapsulation ~~package assembly is encased in~~ comprises a ceramic.

54. (Currently Amended) The package assembly of claim ~~48~~ 51 wherein the encapsulation ~~package assembly is encased in~~ comprises a glass.

55. (Currently Amended) The package assembly of claim ~~46~~ 49 wherein the first module ~~is~~ comprises an integrated circuit.

56. (Currently Amended) The package assembly of claim ~~52~~ 55 wherein the integrated circuit ~~is~~ comprises a physical layer chip.

57. (Currently Amended) The package assembly of claim ~~46~~ 49 wherein the second module ~~is~~ comprises an integrated circuit.

58. (Currently Amended) The package assembly of claim ~~54~~ 57 wherein the integrated circuit ~~is~~ comprises a link layer chip.

59. (Currently Amended) The package assembly of claim ~~46~~ 49, further comprising a resistor having a first terminal coupled to the first conductive surface and ~~further having~~ a second terminal coupled to the second conductive surface.

60. (Currently Amended) The package assembly of claim ~~56~~ 59 wherein the resistor has a resistance of approximately one megohm.

61. (Original) The package assembly of claim 59 wherein the resistor is a resistant film.

62. (Currently Amended) The package assembly of claim ~~46~~ 49, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

63. (Currently Amended) The package assembly of claim ~~58~~ 62 wherein the first ground plane comprises a ground wire of a cable bus.

64. (Currently Amended) The package assembly of claim ~~58~~ 62 wherein the second ground plane comprises a chassis of a computer.

65. (Currently Amended) An integrated circuit package assembly for electrically isolating modules, comprising:

a substrate having a first side and an opposing second side;

a first module having a first and opposing second side, the first module being coupled to the first side of the substrate ~~attached to the first side of the substrate on the first side of the first module~~;

a second module ~~attached~~ coupled to the second side of the first module;

a first conductive surface proximate to the second side of the substrate, the first conductive surface conductively coupled to the first module; and

a second conductive surface spaced apart from the first conductive surface and configured to capacitively couple with the first conductive surface to communicate signals from the first module to the second module. ~~to form a capacitor with the first conductive surface, the second conductive surface being coupled to the second module.~~

66. (Currently Amended) The package assembly of claim ~~61~~ 65, further comprising a dielectric interposed between the first and second conductive surfaces.

67. (Currently Amended) The package assembly of claim ~~61~~ 65, further comprising an encapsulation substantially surrounding the package assembly.

68. (Currently Amended) The package assembly of claim ~~63~~ 67 wherein the encapsulation ~~package assembly is encased in~~ comprises a polymer.

69. (Currently Amended) The package assembly of claim ~~63~~ 67 wherein the encapsulation ~~package assembly is encased in~~ comprises a ceramic.

70. (Currently Amended) The package assembly of claim ~~63~~ 67 wherein the encapsulation ~~package assembly is encased in~~ comprises a glass.

71. (Currently Amended) The package assembly of claim ~~61~~ 65 wherein the first module is an integrated circuit.

72. (Currently Amended) The package assembly of claim ~~67~~ 71 wherein the integrated circuit is a physical layer chip.

73. (Currently Amended) The package assembly of claim ~~61~~ 65 wherein the second module is an integrated circuit.

74. (Currently Amended) The package assembly of claim ~~69~~ 73 wherein the integrated circuit is a link layer chip.

75. (Currently Amended) The package assembly of claim ~~61~~ 65, further comprising a resistor having a first terminal coupled to the first conductive surface and further having a second terminal coupled to the second conductive surface.

76. (Currently Amended) The package assembly of claim ~~71~~ 75 wherein the resistor has a resistance of approximately one megohm.

77. (Currently Amended) The package assembly of claim ~~75~~ 75 wherein the resistor is a resistant film.

78. (Currently Amended) The package assembly of claim ~~61~~ 65, further comprising a first ground plane connected to the first conductive surface, and a second ground plane connected to the second conductive surface.

79. (Currently Amended) The package assembly of claim ~~73~~ 78 wherein the first ground plane comprises a ground wire of a cable bus.

80. (Currently Amended) The package assembly of claim ~~73~~ 78 wherein the second ground plane comprises a chassis of a computer.

81-89. (Cancelled)